Wrocław University of Technology

# Final Work of Selected Problem of Circuit Theory 2008

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**Description**: These instructions give you guidelines for preparing papers for Final Work of Selected Problems of Circuit Theory. In point of work with text you can simply use this document as a template for Microsoft Word 6.0 or later. All text styles are defined and you can select suitable style from the list of current styles. The names of the styles are unique and starts from nick name of the specialization "CEPE" e.g. "CEPE-Title", "CEPE-Author", "CEPE-BodyText" etc. In order to preserve defined styles, references and mark you can cyclically refresh whole document (Select all|F9|). In point of required and accessed contents, the final work should be divided and associated with particular subsection. The detail description you can find below.

The main purpose of the work is to draw up two examples of circuit synthesis using given and possible way of circuit synthesis. At the beginning authors should chose two own immittance functions associated with LC and RC subclasses as follows:

- $F_1(s)$ - chosen own LC function,
- $F_2(s)$ - chosen own RC function,

Selected examples are free and are proposed by authors but have to preserve few conditions.

- immittances should be positive real functions,
- the power of "s" in denominator should not be less than three.

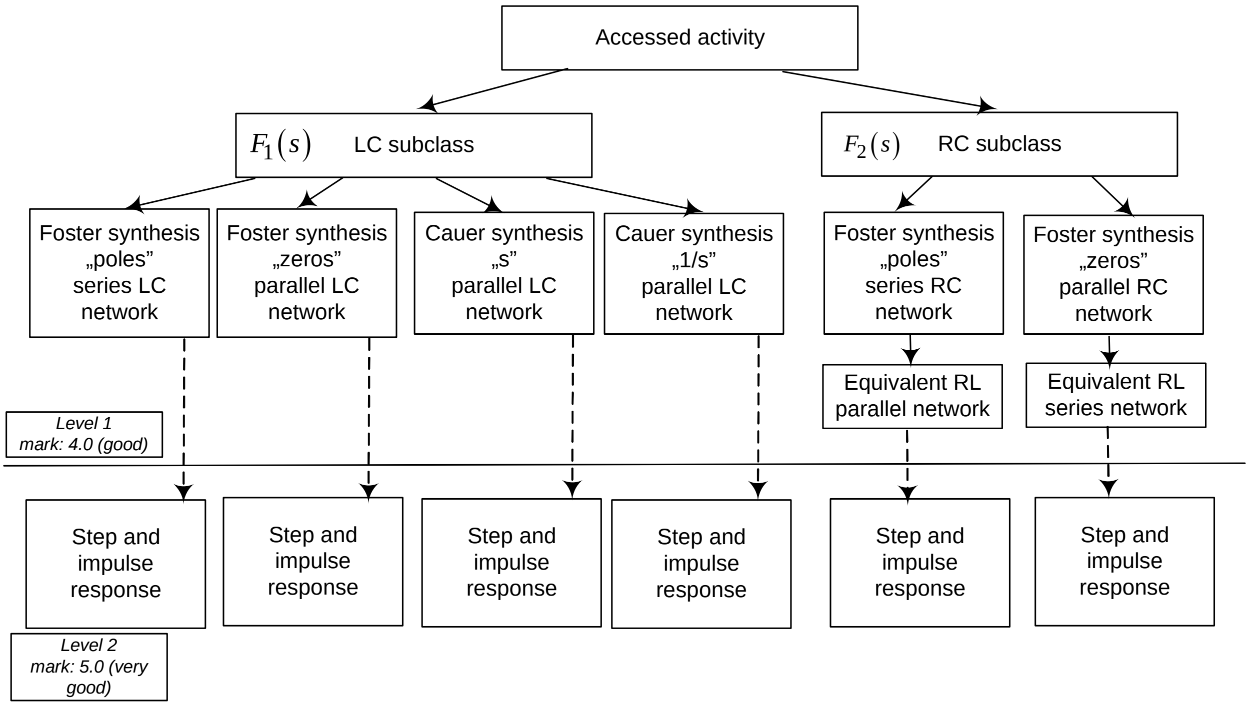


Fig. 0. Characteristic of accessed activity and final mark

Main activities is concentrated around application of discussed during classes method of synthesis. The authors are encouraged to apply all mentioned approach in order to obtain all possible networks which would realize given immittances $F_1(s)$ and $F_2(s)$. Fig. 0 illustrates expectation and main tasks which should be done in order to obtain good (4.0) or very good mark (5.0). The final work, including described below subsections, calculations, parameters and networks is pretending to get good mark. Full version of prepeared work should be sent via e-portal in World format using name specification: *CEPE_SpofCT_FW-Name_Surname.doc*

If additionally author decide to perform computer simulation tests of obtained networks, concentrated here on step response when input is supply voltage and output is main current, it is possible to rise the mark to 5.0. In order to do it authors can apply Matlab environment or Simulink or EMTP-ATP models. Technically, here is additional requirement for the authors to enclose m-files or mdl-files or adp-files to the final work and compressed them using zip or winrar mode with name specification: *CEPE_SpofCT_FW-Name_Surname.zip (rar)*.

Below you can find the description of structure of the final work and expected contents of its sections. Given here description is only for introduce general information and should be delete by authors in final work. Your work should start from section 1 introduction below.

Good luck!
Tomasz Sikorski

## 1. INTRODUCTION

In this section the authors are encouraged to prepare theoretical description dedicated to the problem of circuit synthesis. Direct your attention especially to the issue of zeros and poles localization and its influence on predicted kind of network. Use the references to cited works using square brackets (*Example:* [4]). In case of citation of many works use coma as separator (*Example:* [3], [4]).

## 2. SYNTHESIS OF LC SUBCLASS

Authors should introduce here chosen LC function $F_1(s)$. If you are using Word, use either the Microsoft Equation Editor or the MathType add-on (http://www.mathtype.com) for equations in your paper (Insert | Object | Create New | Microsoft Equation or MathType Equation). "Float over text" should not be selected. You can apply defined text style: "CEPE-Equation". E*xample:*

$$F_1(s) = \frac{s^3 + 2s}{s^4 + 4s^2 + 3} \qquad (1)$$

Present the zeros and poles location of LC function. Inserting figures in the text you can apply defined text style: "CEPE-Figures" and "CEPE-FigureCaption". *Example:*

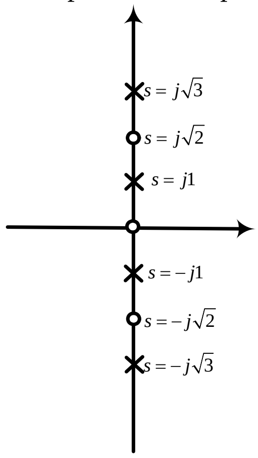


Fig. 1. Location of zeros and poles of LC function $F_1(s)$

### *2.1. Foster synthesis of LC subclass according to poles – series network Z(s)*

Perform here the Foster synthesis according to the poles. Include all calculation of network parameters. *You can adapt below Example*:

$$h_\infty = \underset{s=\infty}{res}\, Z(s) = \lim_{s\to\infty}\frac{Z(s)}{s} = \lim_{s\to\infty}\frac{1}{s}\frac{s^3+2s}{s^4+4s^2+3} = \lim_{s\to\infty}\frac{s^2+2}{s^4+4s^2+3} = \lim_{s\to\infty}\frac{s^2/s^4+2s/s^4}{s^4/s^4+4s^2/s^4+3/s^4} = 0 \Rightarrow L_0 = 0$$

$$h_0 = \underset{s=0}{res}\, Z(s) = \lim_{s\to0} s\cdot Z(s) = \lim_{s\to0} s\cdot\frac{s(s^2+2)}{(s^2+1)(s^2+3)} = 0 \Rightarrow C_0 = 0$$

$$h_2 = \lim_{s^2\to-1}\left(\frac{s^2+1}{s}\cdot Z(s)\right) = \lim_{s^2\to-1}\left(\frac{s^2+1}{s}\cdot\frac{s(s^2+2)}{(s^2+1)(s^2+3)}\right) = \frac{-1+2}{-1+3} = \frac{1}{2} \Rightarrow L_1 = \frac{h_2}{\omega_2^2} = \frac{1/2}{1} = \frac{1}{2}; C_1 = \frac{1}{h_2} = 2 \tag{2}$$

$$h_4 = \lim_{s^2\to-3}\left(\frac{s^2+3}{s}\cdot Z(s)\right) = \lim_{s^2\to-3}\left(\frac{s^2+3}{s}\cdot\frac{s(s^2+2)}{(s^2+1)(s^2+3)}\right) = \frac{-3+2}{-3+1} = \frac{1}{2} \Rightarrow L_2 = \frac{h_4}{\omega_4^2} = \frac{1/2}{3} = \frac{1}{6}; C_2 = \frac{1}{h_4} = 2$$

And finally present the structure of the network. *Example:*

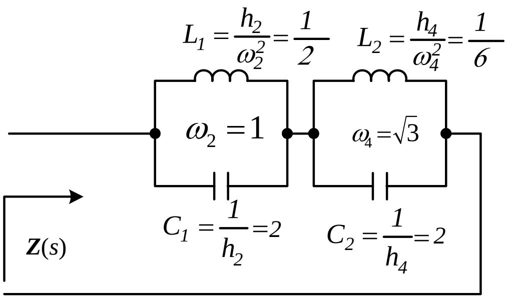


Fig. 2. Final structure of designed network $F_1(s)$ using Foster synthesis according to the poles

### *2.2. Foster synthesis of LC subclass according to zeros – parallel network Y(s)*

If given $F_1(s)$ was realize as impedance you can treat $1/F_1(s)$ as admittance and perform Foster synthesis but now in point of zeros of original $F_1(s)$. Perform the Foster synthesis according to the zeros. Include all calculation of network parameters. *Adapt above Examples of equations and figure captions.*

### *2.3. Cauer synthesis of LC subclass according to "s" – ladder network Z(s)*

Perform here the Cauer synthesis according to the "s". Include calculation of all levels of continued expansion and finally present the network. *You can adapt below Example*:

$$Z(s) = \cfrac{1}{s + \cfrac{1}{\frac{1}{2}s + \cfrac{1}{4s + \cfrac{1}{\frac{1}{6}s}}}} \tag{3}$$

$$\boxed{C_2 = 1, L_3 = 1/2, C_4 = 4, L_5 = 1/6}$$

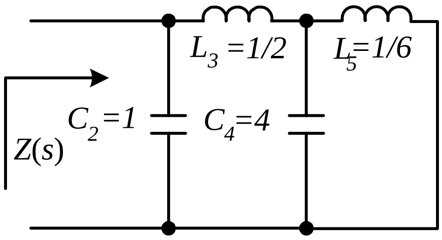


Fig. 3. Final structure of designed network $F_1(s)$ using Cauer synthesis according to "s"

### *2.4. Cauer synthesis of LC subclass according to "1/s" –ladder network Z(s)*

Perform continued expansion according to "1/s". Include calculation of all levels of continued expansion and finally present the network. *Adapt above Examples of equations and figure captions.*

## 3. SYNTHESIS OF RC SUBCLASS

This section is dedicated to realization of RC function $F_2(s)$. Introduce your chosen $F_2(s)$ and present the zeros and poles location of RC function. You can apply defined text style: "CEPE-Figures" and "CEPE-FigureCaption". *Example:*

$$F_2(s)=\frac{s^2+6s+8}{s^2+4s+3} \tag{4}$$

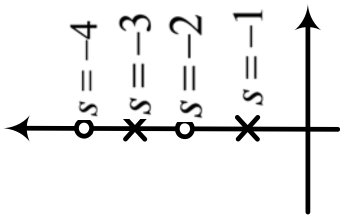


Fig. 4. Location of zeros and poles of RC function $F_2(s)$

### *3.1. Foster synthesis of RC subclass according to poles – series network Z(s)*

Perform here the Foster synthesis according to the poles. Include all calculation of network parameters. *You can adapt below Example*:

$$h_\infty=\lim_{s\to\infty} Z_{RC}(s)=\lim_{s\to\infty}\frac{s^2+6s+8}{s^2+4s+3}=\lim_{s\to\infty}\frac{s^2/s^2+6s/s^2+8/s^2}{s^2/s^2+4s/s^2+3/s^2}=1\Rightarrow R_0=h_\infty=1$$

$$h_0=\lim_{s\to 0} s\cdot Z_{RC}(s)=\lim_{s\to 0} s\frac{(s+2)(s+4)}{(s+1)(s+3)}=0\Rightarrow C_0-\text{ no capacitor}$$

$$h_2=\lim_{s\to -1}\left((s+1)\cdot Z_{RC}(s)\right)=\lim_{s\to -1}\left(\cancel{(s+1)}\cdot\frac{(s+2)(s+4)}{\cancel{(s+1)}(s+3)}\right)=\frac{1\cdot 3}{2}=\frac{3}{2}\Rightarrow C_1=\frac{1}{h_2}=\frac{1}{3/2}=\frac{2}{3};R_1=\frac{h_2}{\alpha_2}=\frac{3/2}{1}=\frac{3}{2} \tag{5}$$

$$h_4=\lim_{s\to -3}\left((s+3)\cdot Z_{RC}(s)\right)=\lim_{s\to -3}\left(\cancel{(s+3)}\cdot\frac{(s+2)(s+4)}{(s+1)\cancel{(s+3)}}\right)=\frac{-1\cdot 1}{-2}=\frac{1}{2}\Rightarrow C_2=\frac{1}{h_4}=\frac{1}{1/2}=2;R_2=\frac{h_4}{\alpha_4}=\frac{1/2}{4}=\frac{1}{6}$$

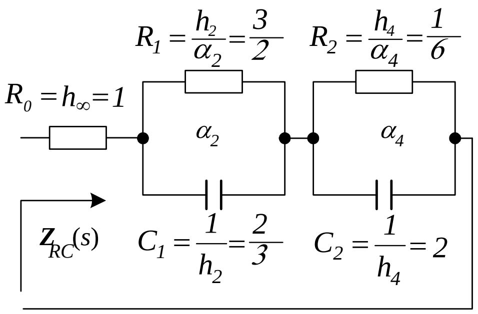


Fig. 5. Final structure of designed network $F_2(s)$ using Foster synthesis according to “s”

### *3.2. Foster synthesis of RC subclass according to zeros – parallel network Y(s)*

If given $F_2(s)$ was realize as impedance you can treat $1/F_2(s)$ as admittance and perform Foster synthesis but now in point of zeros of original $F_2(s)$. Perform the Foster synthesis according to the zeros. Include all calculation of network parameters. *Adapt above Examples of equations and figure captions.*

### *3.3. Equivalent of series RC realization using parallel RL network*

Using the interaction between RC and RL subclass, realize $F_2(s)$ as parallel RL networks

$$Z_{RC}(s) = \frac{s^2+6s+8}{s^2+4s+3} = \frac{(s+2)(s+4)}{(s+1)(s+3)} =$$

$$= 1 + \frac{\frac{3}{2}}{s+1} + \frac{\frac{1}{2}}{s+3}$$

$$h_\infty = 1, \quad h_0 = 0, \quad h_2 = \frac{3}{2}, \quad h_4 = \frac{1}{2}$$

$$H = 1,\ \alpha_1 = 0,\ \alpha_2 = 1,\ \alpha_3 = 2,\ \alpha_4 = 3,\ \alpha_5 = 4 \qquad (6)$$

$$h_\infty = 1 \Rightarrow R_0 = \frac{1}{h_\infty} = 1, \quad h_0 = 0 \Rightarrow L_0 = \frac{1}{h_0} = 0,$$

$$h_2 = \frac{3}{2}, \alpha_2 = 1 \Rightarrow R_1 = \frac{\alpha_2}{h_2} = \frac{2}{3}, L_1 = \frac{1}{h_2} = \frac{2}{3}$$

$$h_4 = \frac{1}{2}, \alpha_4 = 3 \Rightarrow R_2 = \frac{\alpha_4}{h_4} = 6, L_2 = \frac{1}{h_4} = 2$$

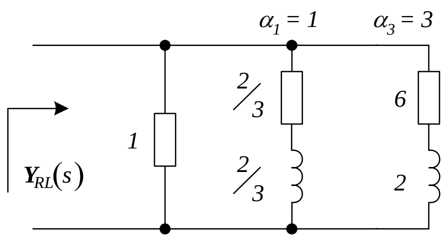


Fig. 6. Equivalent of series RC circuits from subsection 3.1 using RL parallel connections

### *3.4. Equivalent of parallel RC realization using series RL network*

Using the interaction between RC and RL subclass, realize $F_2(s)$ as series RL networks

$$Y_{RC}(s) = \frac{(s+1)(s+3)}{(s+2)(s+4)} = \frac{3}{8} + \frac{\frac{1}{4}s}{s+2} + \frac{\frac{3}{8}s}{s+4}$$

$$H = 1,\ \alpha_1 = 1,\ \alpha_2 = 2,\ \alpha_3 = 3, \alpha_4 = 4$$

$$h_\infty = 0,\quad h_0 = \frac{3}{8},\quad h_2 = \frac{1}{4},\quad h_4 = \frac{3}{8}$$

$$H = 1,\ \alpha_1 = 1,\ \alpha_2 = 2,\ \alpha_3 = 3, \alpha_4 = 4 \qquad (7)$$

$$h_\infty = 0 \Rightarrow L_0 = h_\infty = 0,\quad h_0 = \frac{3}{8} \Rightarrow R_0 = h_0 = \frac{3}{8},$$

$$h_2 = \frac{1}{4}, \alpha_2 = 2 \Rightarrow R_1 = h_2 = \frac{1}{4}, L_1 = \frac{h_2}{\alpha_2} = \frac{1}{8}$$

$$h_4 = \frac{3}{8}, \alpha_4 = 4 \Rightarrow R_2 = h_4 = \frac{3}{8}, L_2 = \frac{h_4}{\alpha_4} = \frac{3}{32}$$

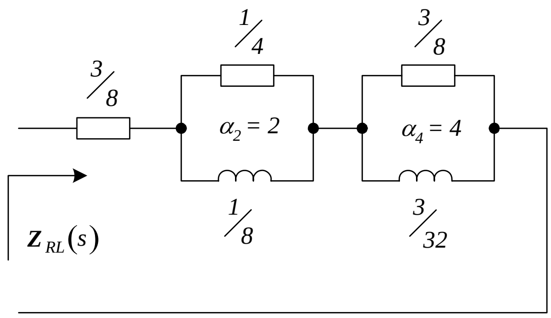


Fig. 7. Equivalent of parallel RC circuits from subsection 3.2 using RL series connections

## 4. COMPUTER TESTS (ONLY FOR VERY GOOD MARK)

Authors who are interested in rising mark to 5.0 have to carried out computer tests of realized above networks, concentrated here on step response when input is supply voltage and output is main current. In this point of view chosen function $F_1(s)$ and $F_2(s)$, which already has been realized as impedance or admittance, can be treated as transfer function “voltage-to-current”. Select two networks: one which realize $F_1(s)$ and second which realize $F_2(s)$. Its up to you which networks you chose from those designed in previous sections. Then, build the model of obtained networks in Simulink or EMTP-ATP environment and carry out the operation of switching on dc supply voltage with amplitude equals 1V with simultaneous record of the main input current. Input is supply voltage, output is supply current. The waveform of supply (main) current is desirable step response.

## 5. REFERENCES

[1] Baker C, Yang Y., *Materials for Circuit Analysis and Synthesis II* http://www.ee.ucl.ac.uk/~yyang/E713.html
[2] Leonowicz Z., *Materials for the lectures on Selected Problems in Circuit Theory*, *http://www.dspace.pl/*
[3] Papoulis A, *Circuits and Systems - A Modern Approach*, Polytechnic Institute of New York, 1980 (selected parts).
[4] Sikorski, T., *Materials for the classes on Selected Problems in Circuit Theory* http://eportal.eny.pwr.wroc.pl/
[5]